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CANCEL 1-13.

14. A thin film transistor array panel for a liquid crystal display comprising:

a gate line formed in a horizontal direction on the insulating substrate,

a gate insulating layer covering the gate line;

a data line formed in a vertical direction on the gate insulating layer;

an align pattern formed on the gate insulating layer and located on both sides of the data line;

~~a semiconductor pattern formed on the gate insulating layer;~~

a drain electrode formed on the semiconductor pattern;

a source electrode formed on the semiconductor pattern, the source electrode being separated from the drain electrode and connected to the data line;

a passivation layer covering the data line, the align pattern, the drain electrode, and the source electrode, and having a contact hole exposing the drain electrode; and

a pixel electrode formed on the passivation layer and connected to the

drain electrod through the contact hole.

15. The thin film transistor array panel of claim 14, further comprising ohmic contact layers formed between the source electrode and the semiconductor pattern, and between the drain electrode and the semiconductor pattern.

16. The thin film transistor array panel of claim 14, wherein the passivation layer and the gate insulating layer have an opening exposing the insulating substrate between the align pattern and the data line.

17. A thin film transistor array panel for a liquid crystal display comprising:

a gate line formed in a horizontal direction on the insulating substrate;

a gate insulating layer covering the gate line;

a data line formed in a vertical direction on the gate insulating layer;

an align pattern formed on the gate insulating layer and located on both sides of the data line;

a semiconductor pattern formed on the gate insulating layer;

a drain electrode formed on the semiconductor pattern;

a source electrode formed on the semiconductor pattern, the source electrode being separated from the drain electrode and connected to the data line;

a pixel electrode formed on the gate insulating layer and connected to the drain electrode and the align pattern; and

a passivation layer covering the data line, the align pattern, the drain

CANCEL CLAIMS 18-19.

20. A thin film transistor array panel for a liquid crystal display comprising:

a gate wire which is formed on an insulating layer and includes a gate line extended in a horizontal direction, and a gate electrode connected to the gate lines;

a gate insulating layer covering the gate wire;

a semiconductor pattern formed on the gate insulating layer;

a data wire, which is formed on the semiconductor pattern, the data wire including a data line extended in a vertical direction, a source electrode and a drain electrode separated from the source electrode and positioned opposite the source electrode with respect to the gate electrode;

an align pattern formed on the semiconductor pattern and located on both sides of the data line;

a passivation layer pattern covering the data wire and the align pattern, the passivation layer having a contact hole exposing the drain electrode and an opening between the data line and the align pattern; and

a pixel electrode formed opposite the drain electrode with respect to the passivation layer, the pixel electrode being connected to the drain electrode via the contact hole.

21. The thin film transistor array panel of claim 20, wherein portions of the pixel electrode and the align pattern overlap to each other.

22. The thin film transistor array panel of claim 20, wherein a distance

between th data line and a boundary of the pixel electrode adjacent to the data line is equal to or greater than a distance between the data line and a boundary of the align pattern adjacent to the data line.

23 The thin film transistor array panel of claim 20, wherein a portion of the align pattern is exposed through the opening.

24. The thin film transistor array panel of claim 23, wherein the pixel electrode is extended on the align pattern and connected to the align pattern.

25. The thin film transistor array panel of claim 24, wherein the opening is extended to the semiconductor pattern and the gate insulating layer, and the insulating substrate is exposed through the opening.

26 The thin film transistor array panel of claim 25, wherein the semiconducior pattern and the gate insulating layer are under-cut under the align pattern adjacent to the data line.

27 The thin film transistor array panel of claim 20, further comprising repair lines overlapping the portion of the data line and the both end portions of the align patterns, respectively, the repair lines being formed on the same layer as the ~~gate~~ wire.

28. The thin film transistor array panel of claim 20, further comprising a supplementary data line formed on the same layer as the data wire, the supplementary data line intersecting the gate line,

wherein both end portions of the supplementary data line are connected to the data line.

. The thin film transistor array panel of claim 29, further comprising a

supplementary data line formed on the same layer as the pixel electrode, the supplementary data line intersecting the gate line,

wherein both end portions of the supplementary data line overlap the data line.

29 . The thin film transistor array panel of claim 28, wherein the gate line includes a first gate line and a second gate line, and a gate connecting portion interconnecting the first gate line and the second gate line.